A

Dissertation Report on

"Three-phase resistive capacitor switching transient limiter for mitigating power capacitor switching transients"

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by

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CERTIFICATE

This is to certify that, Mr. Yuvraj Jaykar Gaikwad (1729005) has successfully completed the dissertation work and submitted dissertation report on "Three-phase resistive capacitor switching transient limiter for mitigating power capacitor switching transients" for the partial fulfillment of the requirement for the degree of Master of Technology in Electrical Power System from the Department of Electrical Engineering, as per the rules and regulations of Rajarambapu Institute of Technology, Rajaramnagar, Dist: Sangli.

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ABSTRACT

This dissertation presents resistive capacitor switching technique for mitigation of power capacitor switching transients. A network is structured with limiting resistors, microcontroller and three phase coupling transformer. A limiting resistors and coupling transformer undergoes an alternative switching during energizing and steady state mode of the network. During the energizing mode of operation capacitor bank charges through the limiting resistors and secondary of coupling transformer remains open. As a result high impedance of primary forces the current to pass through the limiting resistors. In steady state mode of operation secondary of transformer gets short circuited by means of arduino nano and thus limiting resistors gets bypassed. In this dissertation a resistive capacitor switching technique is implemented and results are observed.

Keywords: Coupling transformer, Transients, Resistive capacitive switching.

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ABBREVIATIONS

RCSTL	Resistive Capacitor Switching Transient Limiter
SWG	Standard Wire Gauge
LCD	Liquid Crystal Display
TQFP	Thin Quad Flat Package
CT	Current Transformer
PT	Potential Transformer

Chapter 1

Introduction

1.1 General

An electrical energy is transfered to the consumers from generating stations. Therefore power factor is an important parameter comes into the picture to perform the reliable operation of flow of electrical energy. Most of the connected loads are inductive therefore have low lagging power factor which tends to cause an increase in current and overall active power loss. Therefore for healthy system power factor should be near to unity. Capacitor banks are connected across the load to provide a leading capacitive current. Capacitor banks gives beneficial advantages to power system such as correction of power factor, voltage boost, reduction of system capacity, and reduction of losses in the system.

Before connecting capacitor banks it is essential to calculate the value of capacitance. It's not a simple task to find out the value of capacitance because power factor penalties changes for different utilities. To estimate the essential value of capacitance for improving the current system power factor to a desired power factor, it is essential to know the kVA or kW, power factor of the previous load and the value of power factor that will be achieved. After calculating value of capacitance, capacitor bank is implemented across the load to achieve preset value power factor. Power factor correction panel then switches capacitor banks as per the requirement. Capacitor banks switched ON and OFF several times to feed reactive power and voltage when there is peak load condition occurs. But due to this switching of capacitor, transients will occur in the system.

Transient occurrence during the switching of capacitor bank is a common phe-

nomenon that can occur during energisation of capacitor. During discharging of a capacitor transient does not occurs in system. During energisation, transient produces due to variation in the voltage of system and the voltage of the capacitor. One of the feature of capacitor is that the magnitude of voltage across its terminals cannot change instantaneously. If a system voltage fed to the capacitor then system voltage becomes zero for small interval of time. Because of this an inrush current appears when capacitor energises. After the energisation of capacitor a system voltage gets recovered with the help of charge on the capacitor. Transients are responsible for the equipment failures and premature wear, electromagnetic interference, control equipment failure, high ground potential and reducing the lifespan of capacitor banks.

A several techniques are implemented for the elimination of switching transients which occurs during the energisation of capacitor. One of the technique is, use of surge arresters for mitigation of switching transients occurs during switching of power capacitors. In this technique it is essential to discharge the surge current effectively, an issues occurs during grounding must be considered during the operation. Another methods which are related to zero voltage closing control, energises capacitor bank whenever the value of voltage across switching contactors is nearly zero. These approaches utilise the power electronic devices which tends to implement an extra control system. As a result both cost and complexity of the system increases. An inserting a limiting reactor at the instant of energisation of capacitor bank is one of the technique for eliminating capacitor switching transients. Though this is the simple and less expensive technique there is a problem of series resonance occurrence. Apart from that pre-insertation of resistor or reactor is one of the approach to eliminate the transients, but it is only useful for the high voltage applications.

A transient limiter with symmetrical structure is implemented for the mitigation of transients. This technique significantly remove transients and series resonance. However, comparing with other structures, this technique utilises twice the number of reactors, which tends to increase the cost of system. One of the technique proposed in recent time is inserting a DC reactor for the elimination of transients. Single phase capacitor transient limiter with DC reactor is one of the technique to eliminate the transients. This single-phase device needs to be implemented

separately in three phases, which tends to utilise the more number of the electronic components of the network, as a result reliability of the overall system gets reduces. Apart from that, the imbalance in voltage occurs across the terminals of capacitor bank if a single-device failure occurs, which has adverse effect on the operation and performance of the system. A limiter with single-DC reactor eliminates the transients by providing a large amount of impedance through coupling transformer at the time of energisation.

A reliable and simple structure of transient limiter with resistive capacitor switching, eliminates power capacitor switching transients from system. This technique utilises limiting resistors to eliminate the transients during energisation of capacitor bank. A coupling transformer is implemented to bypass the resistors in steady-state mode of operation. Therefore, the RCSTL network has no considerable effect on the overall system after the energisation of capacitor bank .

1.2 Motivation of the present work

1. Nowadays power factor improvement becomes an essential tool to avoid the penalty from the utilities. As a result capacitor banks are comes into the picture to achieve the power factor to expected value. But capacitance estimation for particular utility is not easy task.

2. Because of awareness regarding power quality problems, customers as well as utilities are showing an interest in implementing different techniques for limiting and controlling of capacitor switching transients.

3. Charging of capacitor bank can produce phase to ground and phase to phase over-voltages at the capacitor bus and also at remote locations.

1.3 Layout of the thesis

To support the performance and implementation of three-phase resistive capacitor switching transient limiter for mitigation of capacitor switching transients. Following contents are proposed in this dissertation work.

1. Importance of RCSTL network.
2. RCSTL with control strategy
3. Design and operation of RCSTL network

4. Design prototype hardware for RCSTL network
5. Conclusion and future scope is presented.

Based on these contents flow the dissertation work is divided into the following chapters:

Chapter 1: Introduction to importance of power factor correction in today's industrial scenario. To achieve the desired power factor at utility as well as at consumer side, present techniques are introduced. Apart from that suitable techniques with their advantages and disadvantages are introduced.

Chapter 2: It provides a detailed literature review about power capacitor switching transient limiters, including different control strategies used for mitigation of capacitor switching transients. Different techniques with their effectiveness and reliability are reviewed to design a cost effective and reliable solution for mitigation of power capacitor switching transients.

Chapter 3: Presents RCSTL network and capacitor selection issues. Introduce control techniques and brief explanation about the RCSTL. Apart from that measuring instruments and network devices with their ratings are introduced in this chapter.

Chapter 4: Operation and implementation of RCSTL network with control strategy is discussed in this chapter. It consists of model of the proposed network with design and working of all circuits. A MATLAB model for the RCSTL is designed with all their parameters.

Chapter 5: This chapter presents results and discussion of simulation and hardware of proposed RCSTL network. Apart from that experimental setup of hardware of RCSTL network is proposed in this chapter.

Chapter 2

Literature review

2.1 Introduction

Nowadays a various industries are implementing an automatic power factor correction panels using capacitor banks for the improvement of power factor, but these capacitor banks are making an issue of switching transients during its energization. To improve the power factor capacitor banks are connected across the load and switched as per the requirement. An uncertain loads and fluctuations in voltage are responsible for the switching of capacitor banks. As a result an unwanted voltage and current spikes having magnitude several times that of voltage and current in steady state will appears in the system, which tends to reduce the life of capacitor banks and electromagnetic switches. Apart from that load equipments connected to the system gets affected. Therefore to suppress these transients from the system certain techniques are implemented.

2.2 Literature Review

2.2.1 Shunt capacitors and power factor correction

To improve efficiency of system and capability of power transfer, shunt capacitors are implemented. Growth rate of capacitor banks is more than that of the growth rate of active power generation. A reactive power is generated by the shunt capacitors to minimize the reactive power flowing in the system. Because of reduction in reactive power, power loss in system is reduced and voltage gets controlled.

Shunt capacitors are installed near to the load .

Some of the benefits of shunt capacitors are as follows:

1. It improves system steady state stability

2. Reduces losses in feeders which minimize the voltage drop, hence provide greater voltage regulation.

3. Due to reduction in voltage drop, torque capability of motor improves.

4. kW and kVA ratings of machines are subsequently reduced.

5. Improves power factor of overall system and thus switchgear wear and tear gets minimized.

An interest in correction of power factor increased because of new recommendations and future standards. 0. Garcia, LA. Cobos, R. Prieto, P. Alou, J. Uceda reviewed solutions for single phase applications. These are classified according to the current waveform of line current, quantity of switches, control strategies, energy processing, etc. Major benefits and dis-advantages are given and applications are discussed [1].

Thomas M. Blooming discusses the issues while applying capacitors. There are a number of application issues taken into the account. These issues are basic as well as complex. Following are some of the parameters taken into account before application of capacitors [2].

1. Capacitor sizing

2. Power factor penalties from utility

3. Ratings of capacitor and selection

4. Harmonics

5. Capacitor switching transients

2.2.2 Techniques for elimination of capacitor switching transients

Dr. Mrs. Hina Chandwani, C. D. Upadhyay, Akil Vahora, Goutam Som proposed that for switching overvoltage protection of capacitor bank circuit breakers surge arresters are applied. As per the existing Medium Voltage, Capacitor bank MATLAB model is implemented to indicate the impact of the surge arrester in minimizing circuit breaker transient recovery voltages and reducing chances of circuit breaker restrikes. Calculations are performed for the energy demand of the

surge arresters. Apart from that overvoltage protection levels of the capacitors for different surge arrester arrangements are evaluated [3].

R. W. Alexander proposed synchronous closing control technique for shunt capacitors. Transient occurrence during energization of shunt capacitor is infamous for their severity. Appropriate instant of energisation when voltage of system becomes equal to the charge on capacitor will reduces inrush currents and overvoltages from the system. [4].

Liu, K.C., Chen, N presents, synchronous closing control technique namely voltage-peak closing method, to minimize inrush currents in shunt capacitors and over voltages appeared. Pre-charged voltages and switch timing for charging a single capacitor bank,three-phase capacitor bank and back-to-back capacitor bank are presented. [5].

S.G. Abdulsalam and W. Xu proposed the application of a sequential switching technique for the elimination of capacitor switching transients. In this technique impedance of grounding is linked at the neutral node of the energised capacitor bank with sequential pole switching in network. To minimise value of voltage across open circuit contact of the capacitor breaker phases, neutral impedance is sized. With the help of computer simulation a theoretical description of the proposed technique is given in the proposed study. Apart from that, to achieve minimal transient over-voltage occurerence due to switching of capacitor neutral impedance, sizing criteria introduced [6].

Larry M. Smith explores the techniques for evaluation of transient currents of capacitor bank, based on ANSVIEEE C37.012-1979, for differen voltages, sizes and configurations of capacitor bank implementation in system. Apart from that, different accepted and applied techniques for controlling substation equipment susceptibility to transients, as well as minimising the value of the transients themselves are discussed [7].

Bhargava, B., Khan, A.H., Imece, A.F., et al. Bhargava, B., Khan, A.H., Imece, A.F., et al., performed a parametric study to find out the impact of pre-insertion inductors for limiting remote over-voltages, i.e. at the extreme point of open ended lines or transformer connected lines in system. The results of the proposed technique indicate that the technique may become completely useless for particular system conditions. So this issue is discussed in terms of the physical phenomena

by the author [8].

Shu-Ting Tseng, Jiann-Fuh Chen, proposed a transient limiter with symmetrical structure. In this technique transients can be effectively eliminated by providing large impedance at the time of capacitor switching, after energisation, for the compensation of power losses from network, the proposed network acts as a short circuit. Theoretical analysis of proposed network in steady state, energization state, and deenergization state have been carried out with selection of the components are given. [9].

Teymoor Ghanbari, Ebrahim Farjah, Amir Zandnia proposed a transient limiter with solid-state capacitor switching. The proposed network works in two modes one is limiting mode and another is bypass mode. DC reactor and a varistor suppress inrush current and transient overvoltage during the capacitor energising and in steady state mode. DC reactor is bypassed by a thyristor, so network acts as short-circuit and has no significant impact on overall system. An auto-triggering technique is used to trigger the thyristor in normal condition [10].

H.-T. Tseng J.-F. Chen proposed a transient limiter along with a half-wave rectifying compensating voltage network. To eliminate capacitor transients at the instant of energisation the proposed network provides a transient inductance. The limiter gives zero impedance depending on the compensating voltage principle after completing restraint, and without requiring any control the capacitor is to be linked directly to the system voltage source. Therefore no over-voltage occurs across the terminals of capacitor in steady state as the capacitor current and voltage wavepaths are not distorted [11].

S.-T. Tseng J.-F. Chen proposed a transient limiter with rectifier for eliminating capacitor switch on transients from the system. The operating conditions are charging suppressive mode and steady state mode with its initial transient respectively. In charging suppressive mode, diode conducts automatically and after that DC reactor provides large impedance to suppress transients at the time of switching on. In steady-state mode with its initial transient, bridge rectifier's diode conduct and limiter freewheels, so proposed limiter works as a short circuit and thus does not have considerable impact on network [12].

Hsu-Ting Tseng and Jiann-Fuh Chen proposed the singled reactor type fault current limiter to eliminate the low voltage transients from system. During steady

state mode, the limiter freewheels and the bias voltage forces all diodes of rectifier to conduct step by step. So, voltage across secondary side of coupling transformer is zero, and primary side of transformer works as a short circuit. In steady state the limiter does not cause rise in voltage at the terminals of capacitor or intrruption of the current waveform of capacitor. [13].

Teymoor Ghanbari, Ebrahim Farjah, Farshid Naseri proposed a resistive capacitor switching transient limiter for elimination of transients. In energisation mode of the capacitor bank, the thyristor remains off and coupling transformer's secondary side acts as open circuit. Consequently, transformer's magnetic reactance in parallel with the limiting resistors and high impedance is inserted in series with the capacitor bank. In this case, the limiting resistors suppress the transients. During steady state mode, thyristors triggered by control system and the coupling transformer works as short circuit. Therefore, the limiting resistors are bypassed by the coupling transformer. Therefore, proposed network has no impact on the circuit [14].

2.3 Closure

The given literature presents different techniques for the mitigation of power capacitor switching transients with different control strategies. These techniques successfully eliminates the switching transients, but there are certain limitations of these techniques such as cost, more number of electronic devices and reactors, response time and control system. Therefore to overcome these limitations a resistive capacitive switching transient limiter with arduino nano is proposed.

2.4 Objectives of present work

In this dissertation work a three phase resistive capacitor switching transient limiter for mitigating power capacitor switching transients is proposed with arduino control strategy. The objectives of work are as follows:

1. To implement resistive capacitor switching transient limiter for the mitigation of power capacitor switching transients with arduino control strategy.

2. To design a single phase coupling transformer to perform the reliable operation of overall system.

3. To design/write a program for the micro-controller for the fast control system response of proposed control system.

Chapter 3

RCSTL Technique and Capacitor selection

3.1 Introduction

RCSTL eliminates the swithing transients from the system with alternate switching betwen limiting resistors and coupling transformer. But before implementing RCSTL for particular system it is essential to perform the mathematical modelling of RCSTL with its equivalent circuit. Apart from that capacitor bank selection and issues related to installation of capacitor bank needs to be analysed for the reliable operation of RCSTL network [2].

3.2 RCSTL network

3.2.1 Working principle of RCSTL network

A RCSTL is based on resistive capacitor switching technique i.e. alternate switching between the two circuits. In energisation mode of capacitor bank one circuit (i.e. limiting resistor) restrains the transients and another remains off. While in steady state mode of operation another circuit (i.e. coupling transformer) comes into the operation and first circuit remains off. As there is alternative switching between two circuits a transients are successfully eliminated with no considerable impact on the overall system.

The concept of limiting resistor and coupling transformer:

1. Limiting resistors

A limiting resistors are used to suppress the transients occurs during the energisation of capacitor bank. A performance of RCSTL network depends upon the limiting resistors. A less value of limiting resistor unable to suppress the transients while greater value of resistor causes power loss therefore value of limiting resistor should be optimum.

2. Coupling transformer

Coupling transformer is implemented to bypass the resistor in steady state mode of operation. A three single phase transformers connected across the limiting resistors to feed the leading capacitive current to the system.

3.2.2 Equivalent circuit of RCSTL

1. Equivalent circuit in energisation mode

Fig. 3.1 shows equivalent single phase RCSTL in energisation mode. The equations of the proposed RCSTL circuit are derived with the help of single-phase equivalent circuit .As three phases of the system are balanced equations for other phases can be easily calculated. As soon as capacitor bank is switched on, the triac remains off until capacitor bank reaches to predetermined amount of charge. R_L is only present in equivalent circuit.

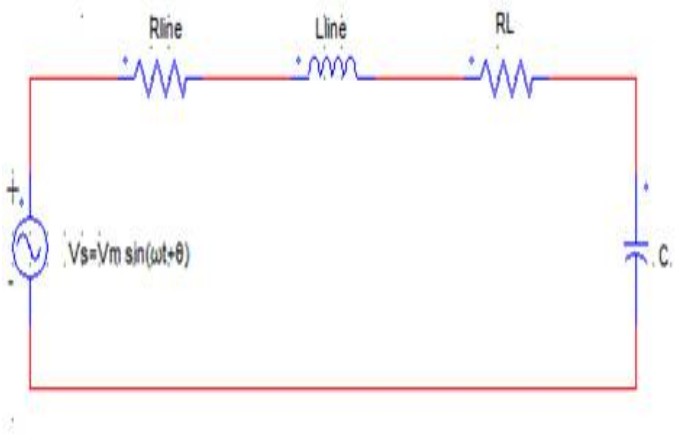

Figure 3.1: Equivalent single phase circuit of RCSTL in energisation mode

Assume that capacitor bank is switched on at $t = t_0$ and the initial parameters are given as

$$V_c(t_0) = V_0 \tag{3.1}$$

$$I_c(t_0) = 0 \tag{3.2}$$

Where,

V_c = Voltage of capacitor bank

i_c = Capacitor bank's current

Differential equation of the circuit in Fig.1 can be derived as

$$(R_{line} + R_L)i_c + L_{line}\frac{di_c}{dt} + V_c = V_m sin(\omega t + \theta) \tag{3.3}$$

$R_(line)$ is very less as compare to R_L therefore it can't be taken into account and current of capacitor bank is given as follows

$$i_c(t) = \frac{V_m}{z_1} sin(\omega t + \theta - \phi_1) + in(t) \tag{3.4}$$

Where, i_n(t) is natural response of circuit and Z_1 and ϕ_1 are given as

$$Z_1 = \sqrt{R_L^2 + \left(\omega L_{line} - \frac{1}{\omega c}\right)^2} \tag{3.5}$$

$$\phi_1 = tan^{(-1)}\left[\frac{\omega L_{line} - \frac{1}{\omega c}}{R_L}\right] \tag{3.6}$$

2. Equivalent circuit in steady state mode

Fig. 3.2 shows the steady-state equivalent circuit of RCSTL. In steady state mode R_L bypassed. Voltage drop across triacs is taken into the account. Therefre $V_t riac$ is added in the equivalent circuit. Equations of the steady state system are given as follows

$$R_{line} * i_c + L_{line}\frac{di_c}{dt} + V_c = V_m sin(\omega t + \theta) - V_{traic} \tag{3.7}$$

Current of the capacitor in steady state mode can be given as follows

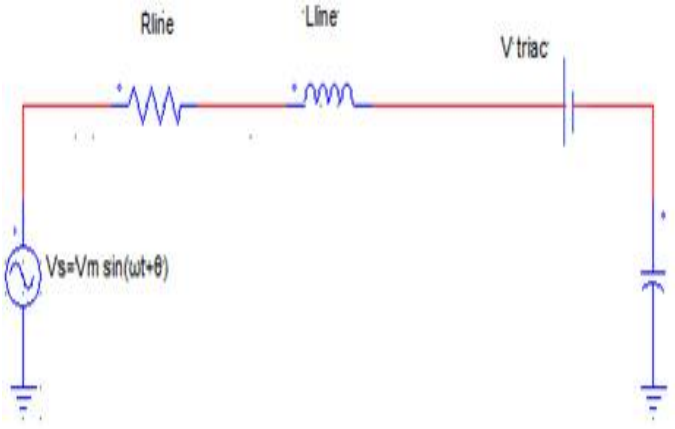

Figure 3.2: Steady state equivalent circuit of RCSTL

$$i_c(t) = \frac{V_m}{Z_2} sin(\omega t + \theta - \phi_2) + i_n(t) \tag{3.8}$$

Where, $i_n(t)$ is the natural response and Z_2 and ϕ_1 are given as

$$Z_2 = \sqrt{R_{Line}^2 + \left(\omega L_{line} - \frac{1}{\omega C}\right)^2} \tag{3.9}$$

$$\phi_2 = tan^{(-1)}\left[\frac{\omega L_{line} - \frac{1}{\omega c}}{R_{Line}}\right] \tag{3.10}$$

3.2.3 Selection of limiting resistor and coupling transformer

1. Limiting resistor

An optimum value of the limiting resistor is selected for suppressing the transient occurs during the energisation of capacitor bank. limiting resistor's value can be evaluated using eq. 3.3 by neglecting R_line and L_line and rewritten as

$$R_L + V_c = V_m sin(\omega t + \theta) \tag{3.11}$$

To find the required value of limiting resistor for eliminating an I_inrush current AC voltage is replaced with DC voltage which is same as that of peak magnitude of V_m. With some manipulations and taking laplace transform optimum value of limiting resistor can be calculated [14] as,

$$R_L = \frac{V_m - V_0}{I_{(inrush,peak)}} \tag{3.12}$$

Where,

V_0= Capacitor bank initial voltage

V_m= Main Source voltage

2. Coupling transformer

Three-phase coupling transformer is configured using three separate single phase transformers. KVA rating of the coupling transformer can be calculated using following formula [13].

$$KVA = \frac{3 * V * I/1000}{Q_C} \tag{3.13}$$

Where,

V = Primary voltage

I = RMS value of line current

Q_c =KVAR rating of capacitor bank

A core area of the transformer is calculated with the help of EMF equation of transformer. An EMF equation of transformer is as follows:

$$E = 4.44 * \phi * f * N \tag{3.14}$$

Where,

f = System frequency

N = Number of turns

We know that,

$$\phi = B_m * A_i \tag{3.15}$$

Where,

B_m = Flux density

A_i = Core area

Therefore by substituting eq.3.15 in eq. 3.14 and re-arranging we get,

$$\frac{E}{N} = E_t = 4.44 * B_m * A_i * f \tag{3.16}$$

Another formula for EMF per turn can be given as

$$E_t = k\sqrt{Q} \tag{3.17}$$

Where,

K = Design factor

Q = Rating of transformer in KVA

From eq. 3.16 and 3.17, core area can be formulated as follows

$$Ai = \frac{k\sqrt{Q}}{4.44 \times Bm \times F} \tag{3.18}$$

A primary and secondary number of turns are same because transformer ratio is taken 1:1. A diameter of the wire can be calculated with the help of current density and current magnitude. A value of diameter is then converted to standard wire gauge (SWG) and required SWG wire is selected from standard values

3.3 Selection of capacitor bank

A capacitor bank consists of two or more capacitors with same ratings and connected in series or parallel with each other. A capacitor bank stores an electrical energy and utilise it for power factor correction or phase shift in AC power supply. Capacitor banks work same as that of single capacitor i.e. to store electrical energy in greater capacity. While going to install any type of capacitor bank there are certain selection methods which help for appropriate selection of capacitor bank. Before going to install capacitor bank for particular system it is essential to find out the issues and parameters associated with it. Following are some of the parameters taken into account before application of capacitors [2].

1. Capacitor sizing

2. Power factor penalties from utility
3. Ratings of capacitor and selection
4. Harmonics
5. Capacitor switching transients

3.3.1 Capacitor sizing

In tariff structure, concerns of power factor issue vary from utility to utility. To seek out the magnitude of capacitance needed for capacitor bank it's essential to grasp KVA or kW, existing power factor and desired power factor. The power factor is calculated as a mean throughout the fifteen or thirty minute interval coincides with the height kW or KVA demand by some utilities. Some utilities calculate the common power factor over the whole amount of months victimization kWh and KVARh over the course of the month.
In past cases to evaluate KVAR, required parameters are power factor, and peak KVA or kW demand over the peak period of time. But, nowadays kWh and KVARh are used to find out the required size of capacitor bank. KVAR calculations are performed at the peak load. It does not matters what should be the value of power factor for lighter and peak load. [2]

3.3.2 Power factor penalties from utility

Power factor penalties are the additional charges applied in electricity bills if power factor is not maintained to pre-set value, typically between 0.8 to 0.9. Penalties are applied according to the customer side power factor. In some cases power factor penalty is hidden. For example, maximum power factor based on kVA demand. In another cases the utility provides an incentives for maintaining power factor above preset value [2].

3.3.3 Ratings of capacitor and selection

Capacitors are designed in such a way that they should tolerate over current and voltages according to their ratings. IEEE Std 18-2002 is the IEEE standard for power capacitors. Continous overload limits given by IEEE Std 18-2002 are as

follows.

•110 % of rated voltage (rms)

•120 % of rated voltage (peak)

•135 % of rated rms current (nominal current based on rated KVAR and voltage)

•135 % of rated reactive power

It is relatively straightforward to select the right amount of kVAR compensation. But, selecting the type of capacitor and actual size is not an easy task. Consumers needs to select the available size, physical and electrical location and type and variability of the load, for proper selection of the capacitor. To find out the type and size of power factor correction equipment some important considerations are stated as follows:

• Penalties

• Payback with installed cost of equipment

• Variations in load

• Losses

• Resonance

• Voltage imbalance

• Load specifications

Above factors can probably cause vital variations in placement and instrumentality choice. [2].

3.3.4 Harmonics

Without discussing harmonics it is not possible to analyze capacitor application issues. Possible effects of harmonics on capacitors are discussed in IEEE Std 519-1992 which are as follows [2].

• Possibility of system resonance is big problem occurs during the usage of capacitors in a power system. Voltages and currents that are imposed by this effect considerably greater than the system working without resonance.

•Reactance of capacitor bank decreases with respect to frequency, thus it acts as a sink for larger harmonic currents. The heating and de-electric stresses are increases by this effect.

• Because of increased heating and voltage stress capacitor life is shortened.

3.3.5 Capacitor switching transients

Transient comes into the picture during the energisation of capacitor. A transient does not occurs during the discharging of capacitor. But during the energisation it may occurs because of the difference betwen voltage of system and capacitor resepectively. A voltage of system becomes zero for a moment i.e. when voltage on capacitor is zero, system voltage is provided to capacitor. Therfore there will be inrush current comes into the picture. System voltage recovered by the charge on the capacitor with same magnitude that it dropped during energisation [2].

3.3.6 Summary

This chapter includes matematical modelling of the RCSTL network in both energisation and steady state mode. Apart from that, issues regarding installation of capacitors are discussed in this chapter

Chapter 4

Configuration of RCSTL Technique

4.1 Introduction

This chapter describes the proposed RCSTL network with control strategy. This chapter includes design of proposed technique in which resistive capacitor switching transient limiter and control system are implemented. Components required for RCSTL network are also discussed in this chapter.

4.2 Development of proposed technique

4.2.1 Configuration of RCSTL network

1. Main proposed system

   A fig. 4.1 shows single line diagram of three phase resistive capacitor switching transient limiter. It consists of three phase coupling transformer, limiting resistors and arduino nano. Three phase coupling transformer obtained from three single phase transformers. Limiting resistors are connected across the transformer and in series with the line. A limiting resistor restrains the transients during the energisation of capacitor bank i.e. in enegisation mode of operation. A coupling transformer's secondary side is connected in star connection and connected to the triac. A triac acts as switch for secondary of the transformer.

A control system consists of current transformer, potential transformer, arduino nano, triac and relays. During the energization of capacitor bank a current flows through the limiting resistor and secondary of transformer is open. A control system kept secondary of the transformer open until the capacitor bank gets charged. After the energization of the capacitor bank secondary of the coupling transformer gets short circuited by means of triacs and thus the system runs in the steady state. A arduino nano will provide the instructions to the triac when capacitor bank gets fully charged. A current transformer and potential transformer are used for the measurement of current and voltages in the system. The measured values are sampled and given to the micro-controller. A LCD display is connected with arduino nano to display the status of operation, current and power factor of overall system.

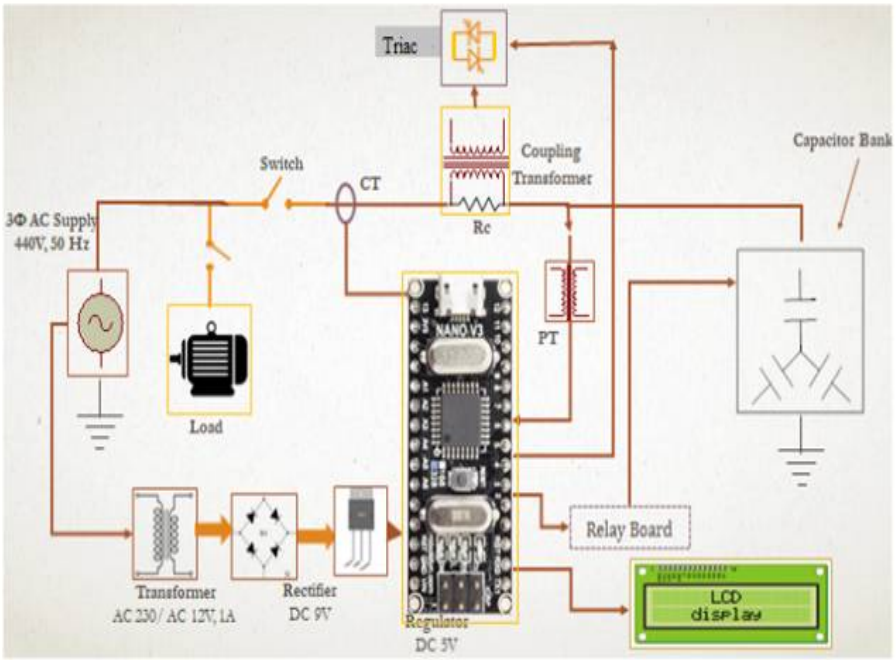

Figure 4.1: Single line diagram of RCSTL network

2. Connections of Micro-controller in arduino nano

A fig. 4.2 shows the connections of micro-controller. A current and voltage measured by CT and PT respectively and sampled. Digital signals then provided to the micro-controller for the further calculations as per the program. For working of controller a 5V DC supply is generated with the help of recti-

fier as shown in fig. 4.2. Control signals generated by the micro-controller are given to the relays and triac for the switching operation. A LCD display is connected along with micro-controller to display the status of network, power factor and current.

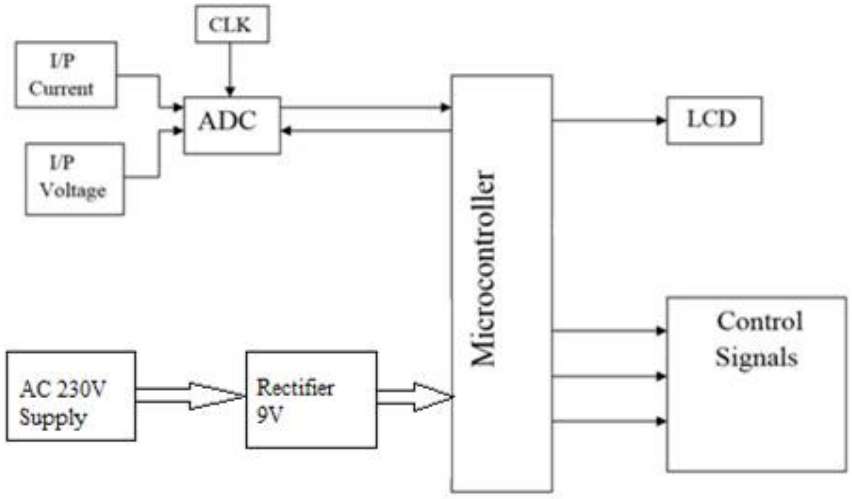

Figure 4.2: Connection of Micro-controller

4.2.2 Simulation model of RCSTL

A RCSTL implemented in MATLAB simulink to observe the performance of network and behaviour of current. MATLAB model of proposed technique is implemented as single phase as well as three phase RCSTL network.

1. Single phase RCSTL network

   A resistive capacitor switching transient limiter is simulated using MATLAB simulink. In MATLAB model of single phase network, a coupling transformer, limiting resistor, capacitor and circuit breaker with controller is implemented. A triac triggered by means of controller for the operation of resistive capacitor switching transient limiter network.

   Fig. 4.3 shows simulation of single phase RCSTL network. In the simulation model one transmission line is connected with the load having the capacitor. A parallel combination of transformer and limiting resistor is implemented to remove the transients and run the system at steady state mode. When the capacitor starts to energize a current is flowing through the capacitor,

which is observed in the simulation result. Current transient appears during the energization of the capacitor. As soon as capacitor gets fully charged a control system will turn ON the triacs and short circuit the secondary of coupling transformer. Therefore the transients are eliminated by the resistor and transformer will bypass limiting resistor after the energization of capacitor, to run the system at steady state mode. A limiting resistor value is selected to optimum to avoid the power loss in the system and to remove switching transients.

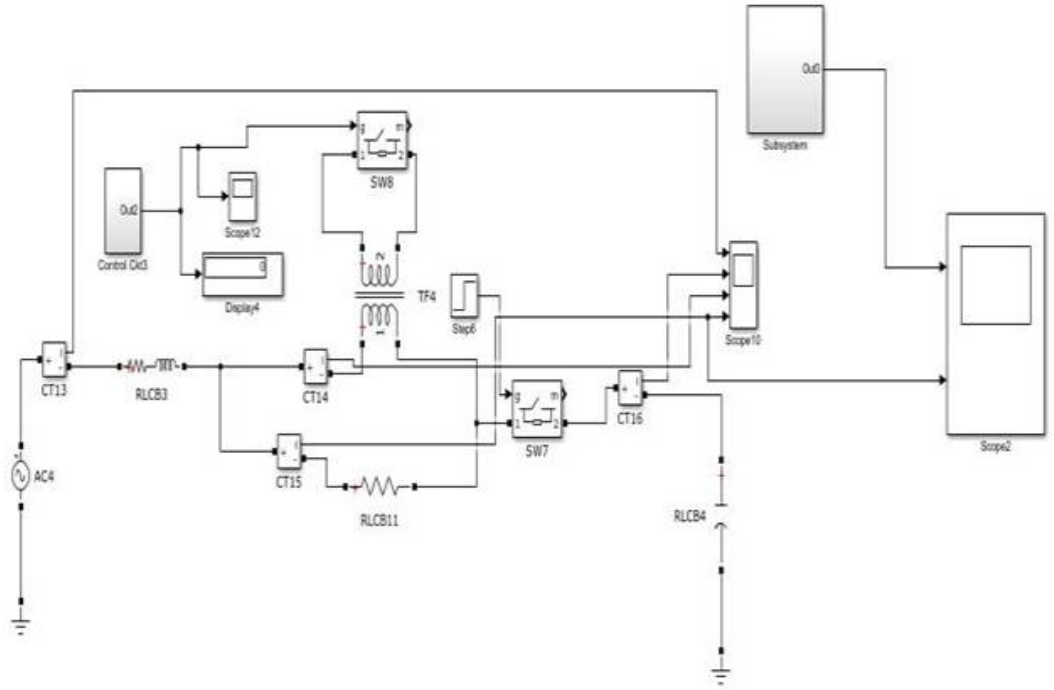

Figure 4.3: simulation of single phase RCSTL network

2. Three phase RCSTL network

A figure 4.4 shows simulation of three phase RCSTL network. An alternative switching between the limiting resistor and coupling transformer is performed by ideal switches connected in the model. Transmission line is connected as load to observe the performance of the system. A step signal is provided to run the system in energizing and steady state mode respectively. A power factor measurement block is connected in the network to measure the initial and improved power factor. A step signals are generated for the operation of

ideal switches connected in the network.

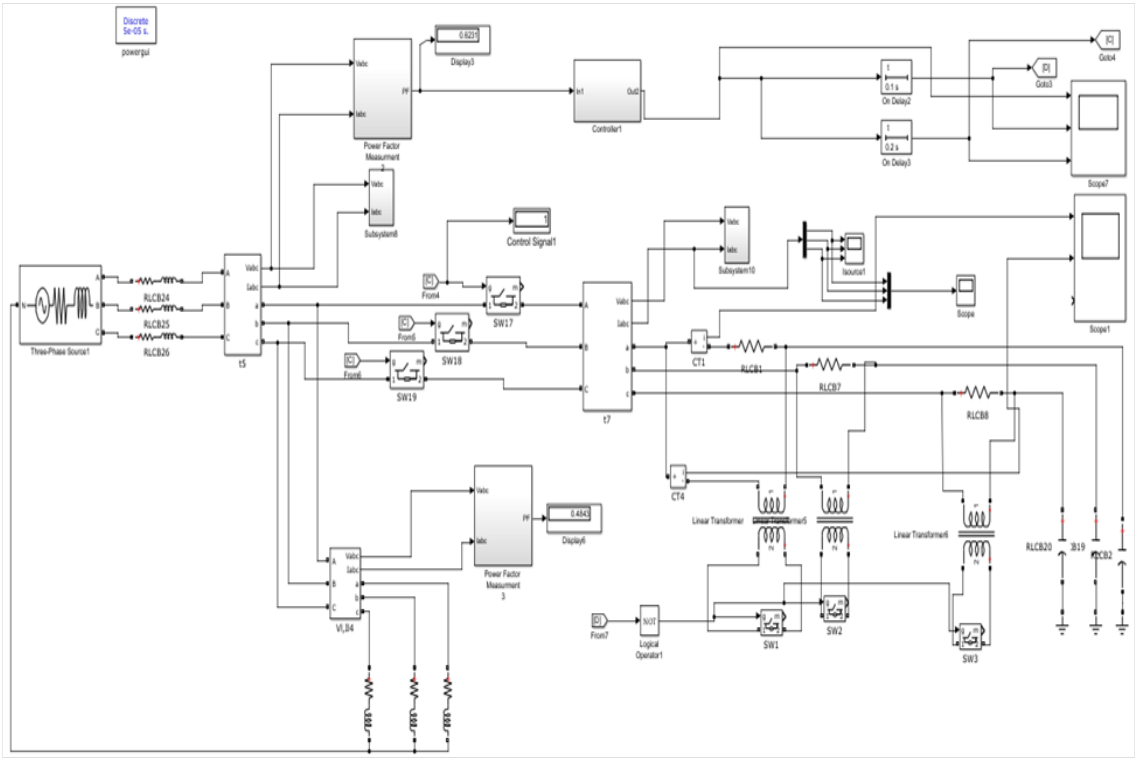

Figure 4.4: Simulation of three phase RCSTL network

4.3 Specifications of components

1. Coupling transformer

   Coupling transformer is constructed with three single phase transformers. From EMF equations of transformer an area of core can be calculated. According to the area, bobbin size is decided from available sizes. A flux density, current density and design factor values are taken from the standard range of values. A table 4.1 shows all the specifications of the coupling transformer.

Table 4.1: Specifications of single phase coupling transformer

Specifications	Value
Transformer rating	0.333 KVA
Secondary voltage (Vs)	110 V
Secondary line current (Is)	3.0273 A
Primary voltage (Vp)	110 V
Primary line current (Ip)	3.0273 A
Number of phases	1 Phase
Maximum flux density (Bm)	1.08 Wb/m2
Current density	3.8 A/mm2
Design factor (k)	0.6
EMF per turn (Et)	0.3462
Turns per volt	2.8882
Net core area (Ai)	1444.1
Available lamination/Bobbin size	6 1"
Width	38.1mm
Length/Stack	38.1mm
Width of window	25.4mm
Height of window	76.2mm

A primary and secondary number of turns are same because transformer ratio is 1:1. A diameter of the wire can be calculated with the help of current density and current magnitude. A value of diameter is then converted to standard wire gauge (SWG) and required SWG wire is selected from standard values. Table 4.2 shows wire specifications.

Table 4.2: Wire specifications

Primary/Secondary number of turns	322
Calculated diameter in mm	1.0074
SWG in mm	1.01
No. of layer	11

2. Arduino nano

A surface mount version with integrated USB port as shown in fig. 4.5 is known as arduino nano. It is a, breadboard friendly, complete and smallest. It has onboard +5V AREF and 8 analog input pins. Power jack is not available in arduino nano. Sensing is done automatically by nano and switch to

the maximum positive voltage source of power.

With the Basic Stamp arduino nano got a pin layout that works well (RX, TX, ATN, GND on one top layer, power and ground on the other). This version has 8-bit AVR ATMega328 microcontroller which is brain of this chip. There is more programming offered by Atmega328P with data memory space. Table 4.3 shows input output ports of arduino nano.

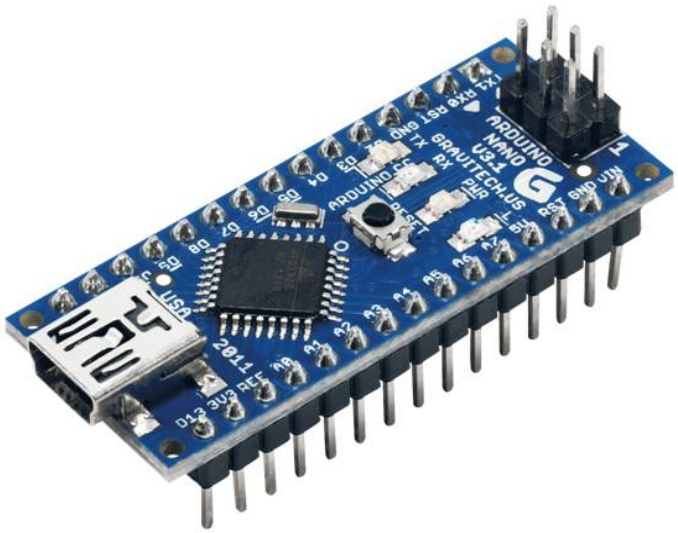

Figure 4.5: Arduino nano

Table 4.3: I/O ports of arduino nano

Pin Number	Name	Type	Explanation
1 to 2, 5 to 16	D0 to D13	Input/Output	Digital i/o port 0 to 13
P3 and P28	RESET	PWR	Reset
P4 and P29	GND	O/P	Provide ground
17	3V3	I/P	Provide 3.3V output
18	AREF	I/P	Reference of ADC
Pin19 to Pin26	A0 to A7	I/P	Analog i/p channel 0 to 7
27	+5V	O/P	Provide 5V output
		Or I/P	or +5V (input from external power supply)
30	VIN	PWR	voltage supply

3. LCD

Fig. 4.6 shows the liquid crstal display which availble in different sizes 2x10,

1x8, 2x8, 1x16, 2x20, 2x16, 4x16, 4x20, 2x24, 2x30, 2x32, 2x40 etc . Special kind of lcd's to be used in products are manufactured by different companies. Same functions (display characters) are performed by all led's.

Figure 4.6: LCD

4. Current Transformer

   Fig. 4.7 shows the construction and symbol of current transformer. In current transformer current of secondary, in normal conditions of use, is substantially proportional to the primary current.

   A CT intended to supply integrating meters, indicating instruments and similar apparatus.

   In electrical system, for estimation of electric current the current transformer (CT) is used. When magnitude of current in circuit is too high to apply for measuring equipments then the current transformer produces a low magnitude current which is appropriately proportional to the current in the circuit..

   CT allows microcontroller to monitor AC Current drawn on a line for PCB. Simple Current Transformer with a 1000/1 ratio. Measures current up to 30A maximum current.

   I/P current: 30A

   O/P current: 30mA

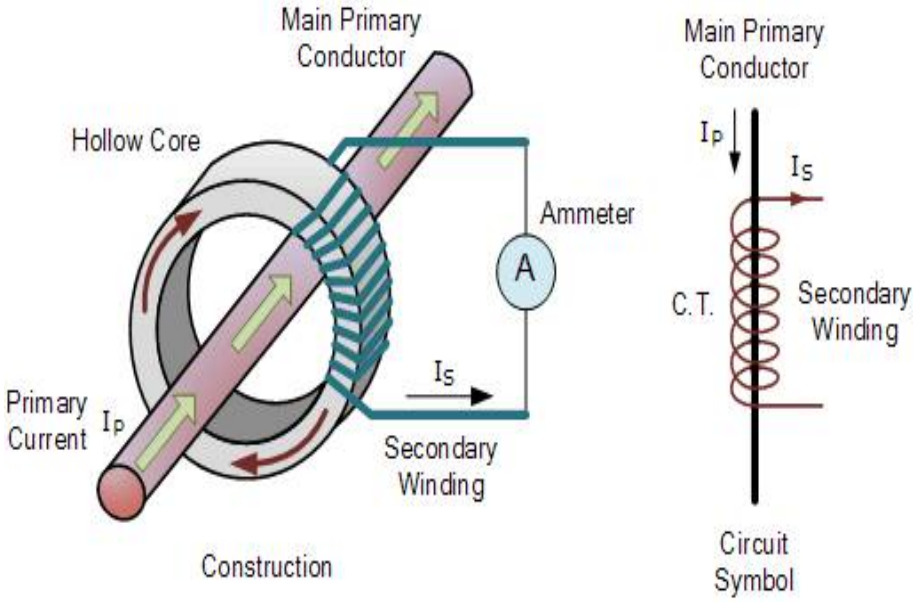

Figure 4.7: Current transformer

5. Bridge Rectifier

Fig. 4.8 shows bridge rectifier. A diode rectifier produces DC supply from AC supply to provide the power to electronic components in the circuit. Rectifiers are used in lots of AC power devices like welding applications, hose equipments, modulation process, controllers of motor, etc.

Bridge rectifier converts AC voltage to DC voltage. Bridge Rectifiers are used on large scale where wide range of DC supply is required. Bidge rectifiers are constructed with the help of four or more than four diodes or with other controlled switches .

As per the current requirement diode rectifier is selected. Before selecting a rectifier some factors are taken into account like ratings of Components and specifications, range of temperature, mounting requirements, current rating of transient, rating of forward current, breakdown voltage etc.

• Types of Bridge Rectifiers

Based on following factors bridge rectifier are classified into several types: bride circuit's configurations, type of supply, controlling capability etc. Bridge rectifiers are categorized into three phase and single phase rectifier resepec-

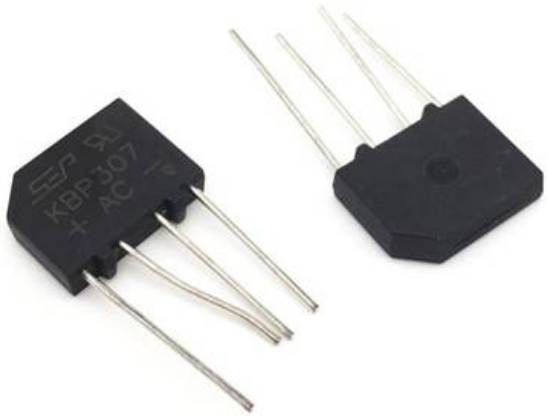

Figure 4.8: Bridge rectifier

tively. These types are further categorized into uncontrolled, full controlled and half controlled rectifiers.

6. LED

Fig. 4.9 shows LED which come in dozens of different shapes and sizes as they are very common. LED's are simple because unlike other chips that have lots of pins with special uses and names, LEDs have only two wires. First wire is the positive (anode) and another is negative (cathode). From two terminals of LED one goes to negative terminal of voltage and the other goes to positive terminal of voltage.

Features:

- The larger lead goes to positive voltage terminal
- Direction of current is from positive to negative
- LEDs does not operate in reverse mode

A forward rated current of LED is 20mA and forward voltage is 2.0V.

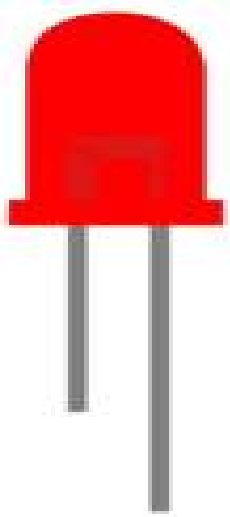

Figure 4.9: LED

Specification:

- Forward drop of 1.8-2.2V
- Current limit of 20mA
- optimum current: 16-18mA

7. Trimpot

Fig. 4.10 shows trimpot which works as a potentiometer. It is used for tuning, calibration and adjustment. Trimpots are adjusted by using a screwdriver and normally mounted on printed circuit boards. With the help of multi turn setting trimpots achieve high resollution and designed for occasional adjustment. If trimpots are used as replacement for potentiometer then it should be taken into account that, they are constructed only for lifespan of 200 cycles.

Different versions of trimpots are available, using adjusting orientations (top, side) and different mounting methods (through hole, smd). single and multiturn variations of trimpots are available.

Figure 4.10: Trimpot

8. Voltage Regulator

Fig. 4.11 shows the basic L7805 voltage regulator. It is designed to achieve the constant voltage. It has three terminals with 5V output. A voltage regulator provides control on thermal shutdown, local regulation, risk free area protection for project internal and current limiting. A maximum current of each one of these voltage regulators can be 1.5A.

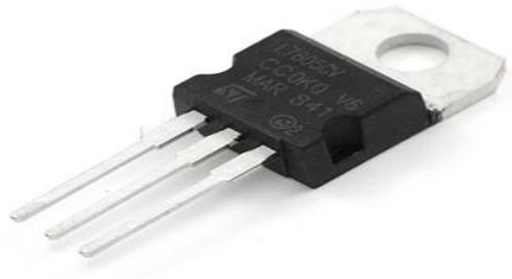

Figure 4.11: Voltage Regulator

9. Potential transformer

Fig. 4.12 shows Potential transformer. Potential transformer is a step down transformer which step down high magnitude of voltage to low measurable voltage. Turns ratio of the PT are very accurate. Potential transformers are connected in parallel with the line whose voltage is to be measured. It has large number of primary turns and less number of secondary turns.

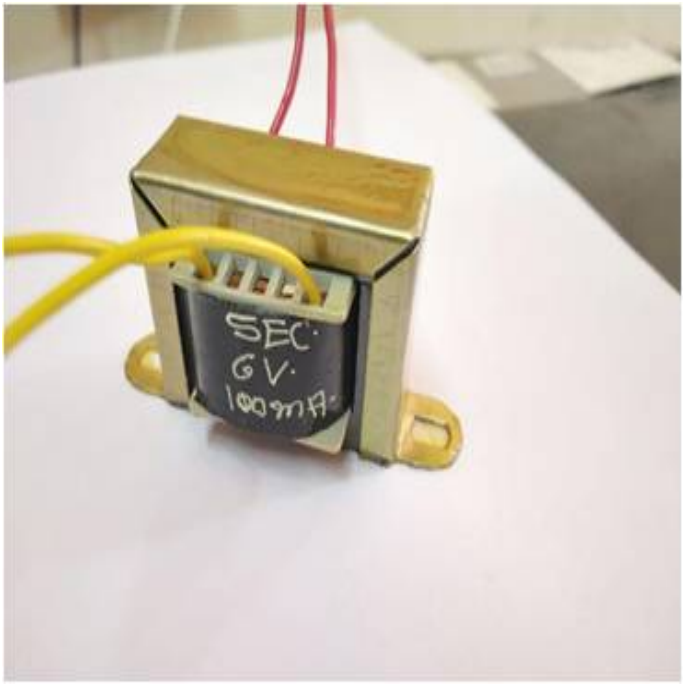

Figure 4.12: Potential transformer

Specifications:

- Input voltage: 230V
- Output voltage: 6V
- Output current :100mA

The pin explanation of the 7805 potential transformer is described in the table 4.4:

Table 4.4: Pin description of 7805 potential transformer

Pin Number	Pin	Explanation
1	I/P	Positive unregulated voltage is given in regulation at this pin in IC
2	Ground	Function of this pin is to provide ground.
3	O/P	At this pin the 5V regulated output is taken out

4.4 Summary

In this chapter along with block diagram, working of the RCSTL network is discussed. Apart from that MATLAB model of the proposed technique is implemented. A description of all components is given in this chapter.

Chapter 5

Results and Discussion

5.1 Results of simulation

Fig. 5.1 shows waveforms of single phase RCSTL network. A transient occured during the energisation of capacitor bank has 2A at the instant of 0.5 second. This transient is then restrained by the limiting resistor and system runs in steady state mode.Therefore, from fig. 5.1 it is clear that, RCSTL successively eliminates the capacitor switching transients.

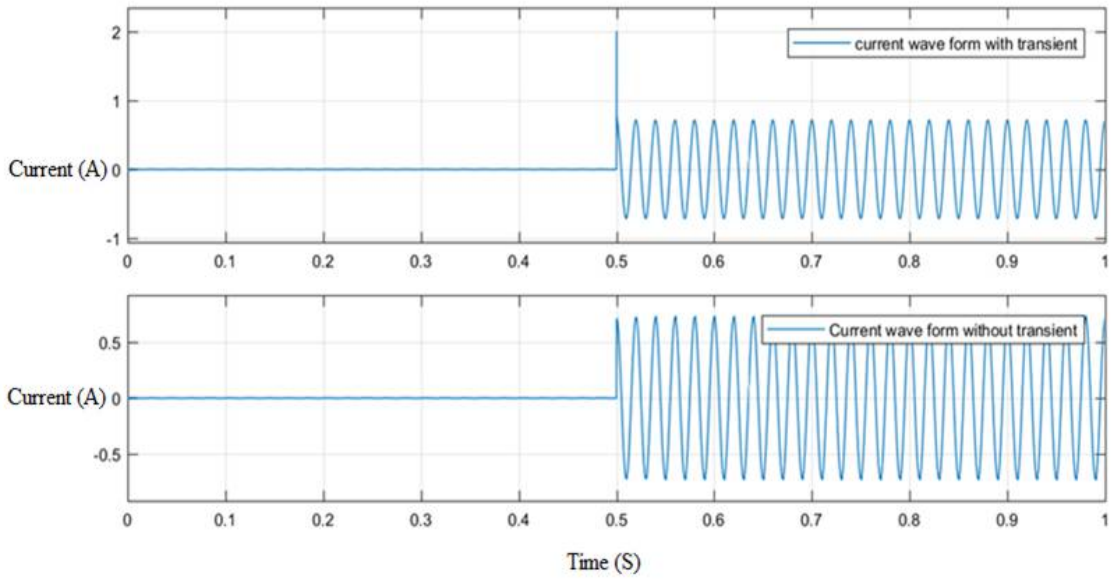

Figure 5.1: Waveforms of single phase RCSTL network

Fig. 5.2 shows waveforms of RCSTL in energisation mode for each phase. During the energisation of capacitor bank transients are occured in all three phases of the system with different magnitude. A waveforms start to distort from 0.2 second. A settling time of waveform is different for different phases.

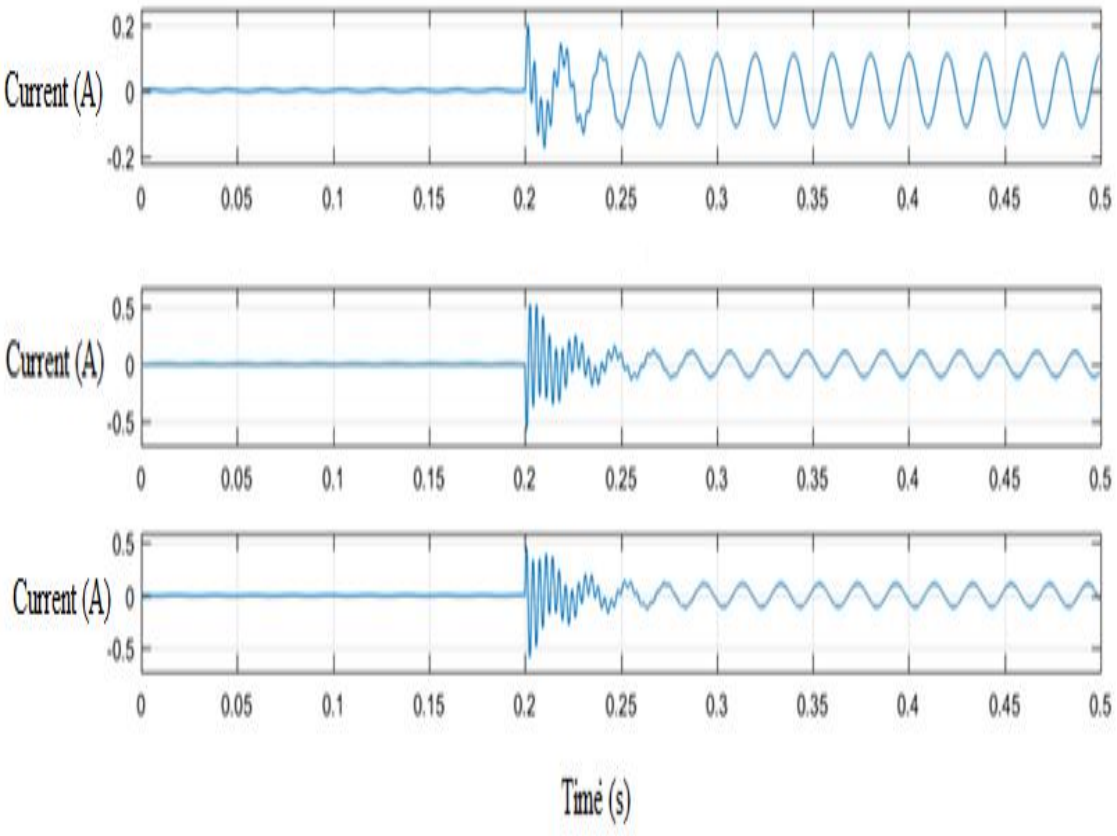

Figure 5.2: Waveforms of RCSTL in energization mode (each phase)

Fig. 5.3 shows waveforms of RCSTL in steady state mode for each phase.After the energisation of capacitor bank current flows through the secondary of coupling transformer, i.e. system runs in steady state mode.Therefore waveforms are transient free. Waveforms obtained are 120 degree apart from each other i.e. three phases are balanced.

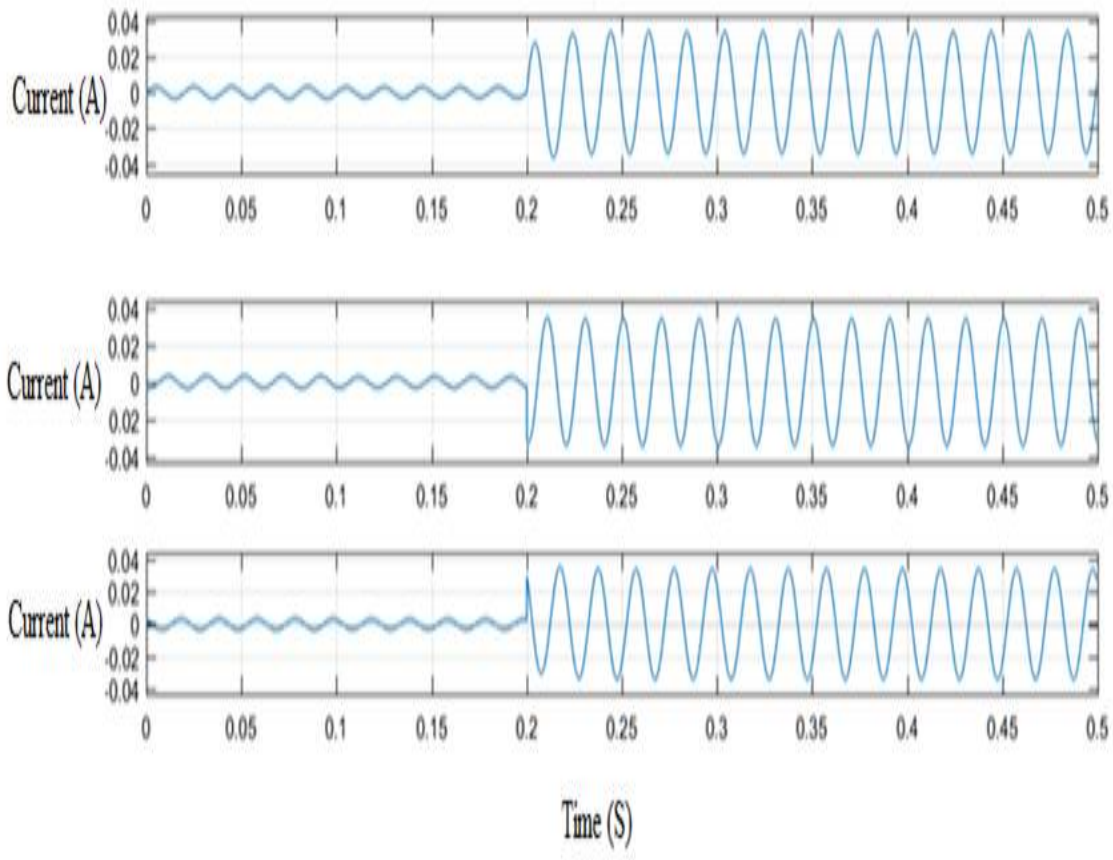

Figure 5.3: Waveforms of RCSTL in steady state mode (each phase)

Fig. 5.4 shows the waveforms of RCSTL in energisation mode for three phase system. At the instant of switching waveforms of the current gets distorted. But settling time is different.

Fig 5.5 shows waveforms of RCSTL in steady state mode for three phase system. At the instant of 0.2 second transient occurs during the energisation of capacitor bank are successively eliminated.

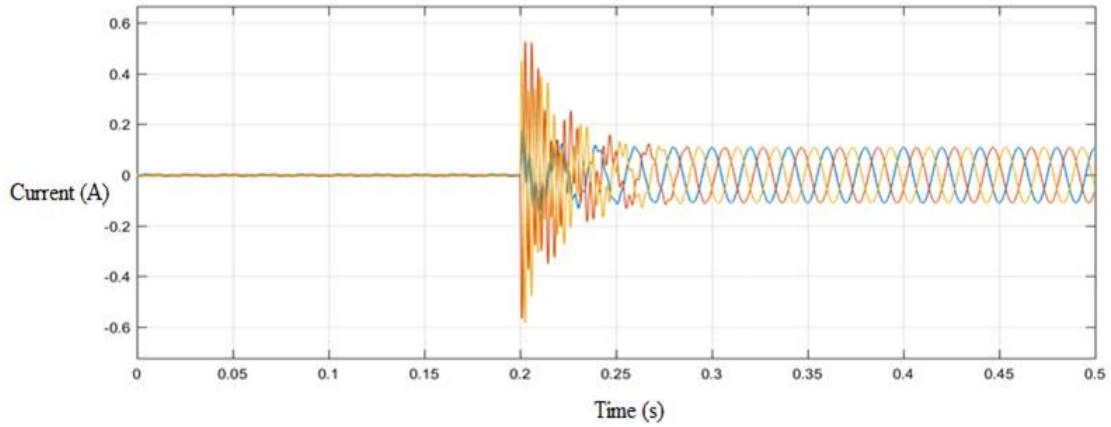

Figure 5.4: Waveforms of RCSTL in energization mode (three phase)

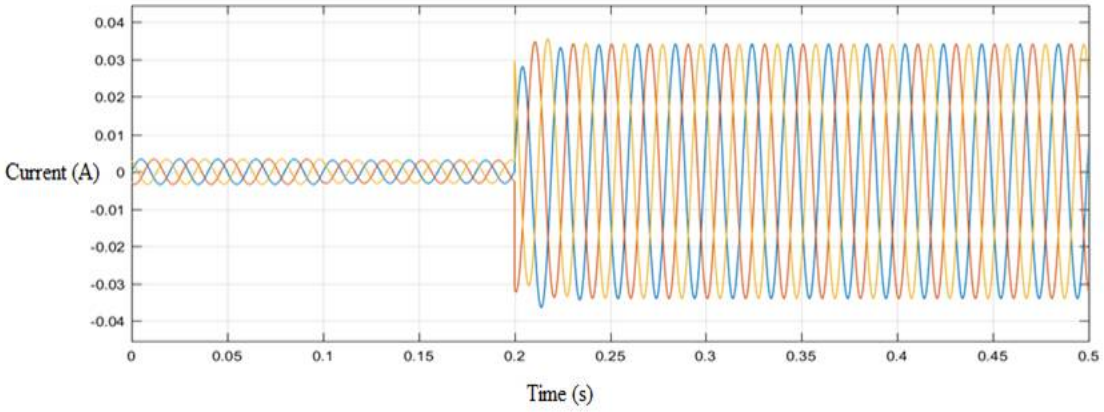

Figure 5.5: Waveforms of RCSTL in steady state mode (three phase)

5.2 Hardware description and results

5.2.1 Operation of RCSTL

There are two modes of operation in resistive capacitor switching transient limiter technique.

1. Energization mode

   Fig 5.6 shows the resistive capacitor switching transient limiter in energization mode. In the energization mode, transients are eliminated by means of limiting resistors and capacitor bank gets energised. A microcontroller programmed for RC time constant i.e. for RC time instant a current should flow through the limiting resistors. At the same time secondary of the coupling transformer kept open by arduino nano with the help of triacs. As a result large impedance of core magnetizing reactance transfered to the primary of coupling transformer. Therefore capacitor bank charged through limiting resistors by removing the transients.

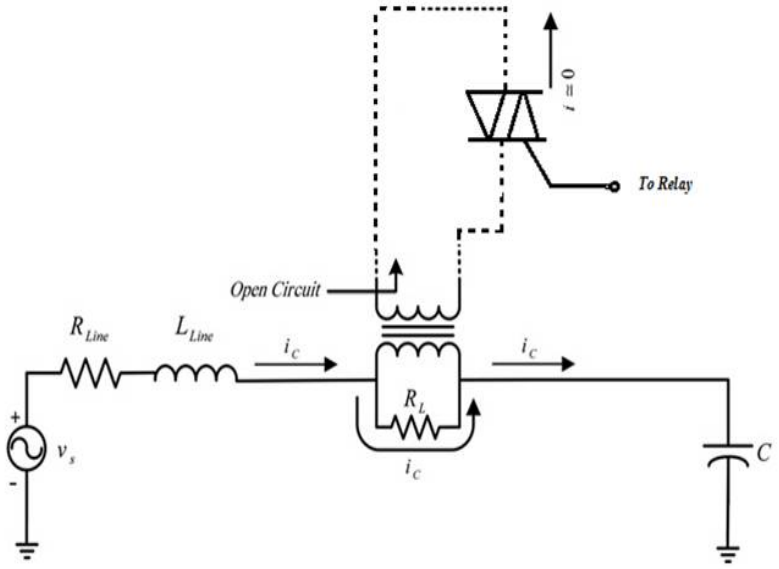

Figure 5.6: RCSTL in energistation mode

2. Steady state mode

   Fig. 5.7 shows RCSTL in steady state mode.After the energization of capacitor bank a secondary of coupling transformer gets short circuited using triac

and diode rectifier. As a result impedance of primary winding of transformer is less than that of the limiting resistor, so it has no impact on the system and system will operate at steady state mode. An arduino nano so programmed to give the signal to the triac after the RC time completed for the energization process. In steady state mode of operation limiting resistors are isolated from the system and thus there is no significant impact of resistive capacitor switching transient limiter on overall system.

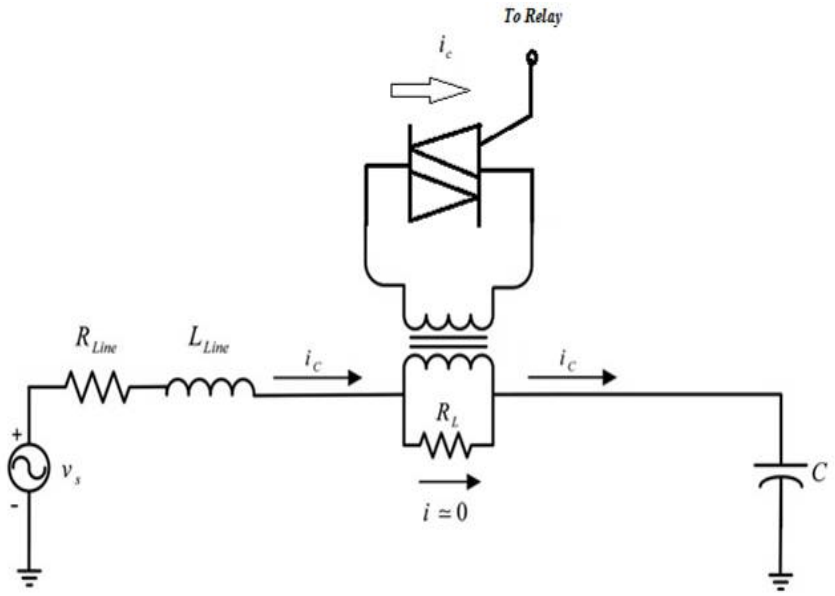

Figure 5.7: RCSTL in steady state mode

5.2.2 Hardware description

Fig. 5.8 shows hardware of three phase RCSTL network. A 5 Hp induction motor connected as a load in the resistive capacitor switching transient limiter network. A capacitor bank connected across the load takes around 3000msec to charge. A capacitor bank is charged through the limiting resistors and thus transient gets suppressed. A highest inrush current during the charging of capacitor bank is 2.075A. A arduino nano displays the current, voltage and power factor during the charging and steady state mode of operation. Power factor of induction motor is improved from 0.79 to 0.86 with successful elimination of transients. A network does not have any impact on the overall system so it is a reliable network to mitigate switching transients.

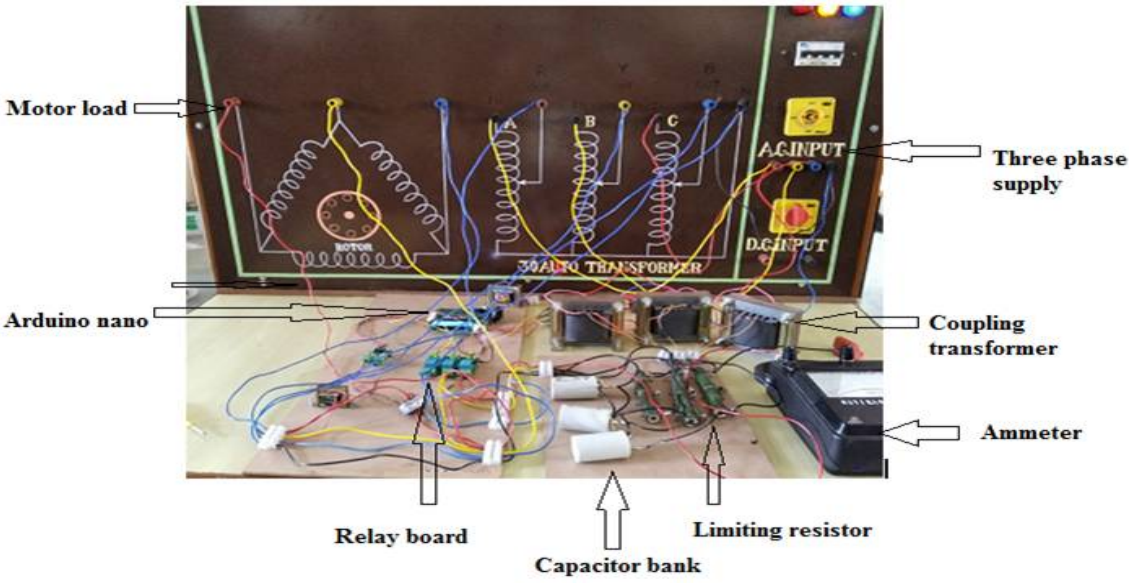

Figure 5.8: Hardware of three-phase RCSTL network

A three phase resistive load of 2.4kW is connected in four steps. Intially 600W load is connected, because of the resistive load power factor is unity. As power factor is unity arduino nano does not connects RCSTL in the circuit. After connecting a 1200W load arduino actuate relays and RCSTL gets connected into the system. After that capacitor bank gets charged through the limiting resistors with the same load because charging time is 3000msec. After charging of capacitor bank coupling transformers comes into action to run the system at steady state mode. A 1800W and 2400W loads connected resepectively and power factor is observed. Fig. 5.9 shows load vs power factor characteristics of RCSTL netwok. Power factor is unity for 600W load initially. Due to addition of a reactance of coupling transformer power factor gets reduced for 1200W load. For 1800W and 2400W load a power factor improves because a leading capacitive current is provided by the capacitor bank.

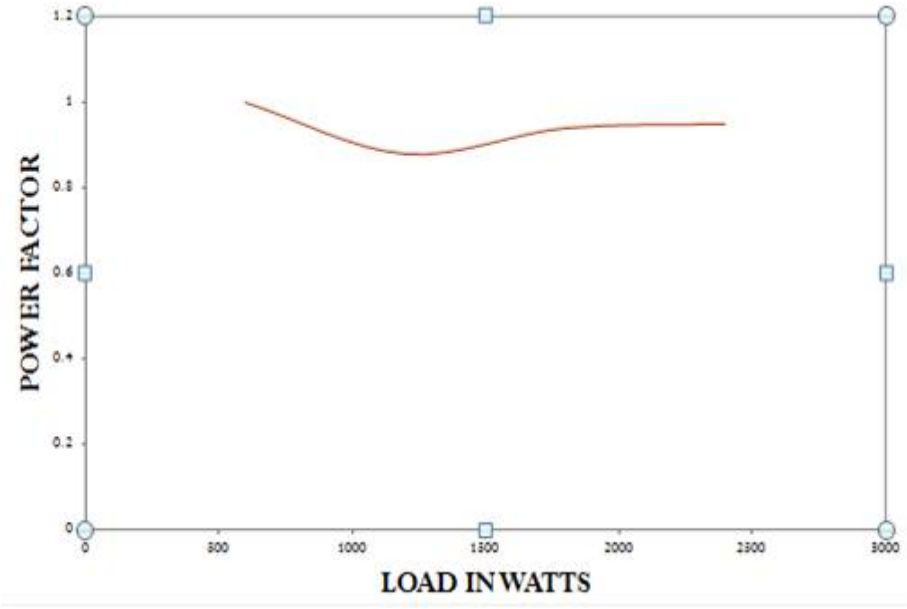

Figure 5.9: Load vs power factor characteristics of RCSTL network

Fig 5.10 shows load vs current characteristics of RCSTL network. A current is gradually increases with respect to load.

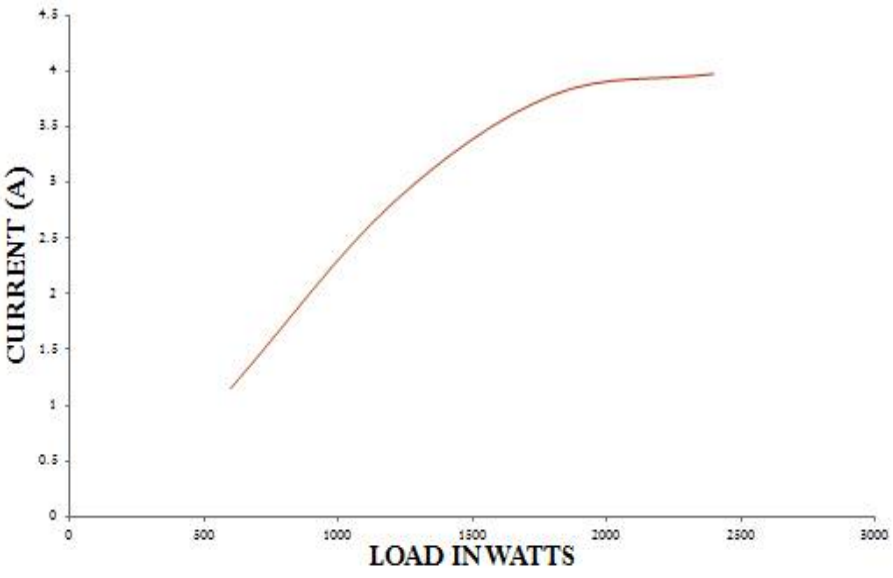

Figure 5.10: Load vs cureent characteristics of RCSTL network

Fig. 5.11 shows load vs voltage characteristics of RCSTL network. A voltages gradually decreases with respect to load.

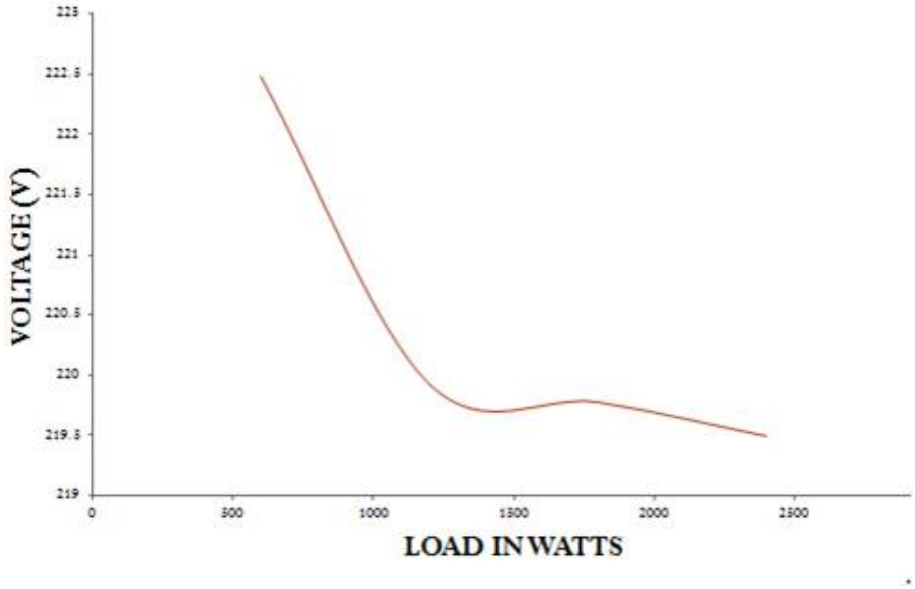

Figure 5.11: Load vs voltage characteristics of RCSTL network

5.3 Summary

In this chapter simulation results are given, from which it is clear that the RCSTL successively eliminates the transients during the charging of capacitor bank. A MATLAB results of RCSTL network are shown in this chapter. Apart from that a hardware results are observed and discussed in this chapter.

Chapter 6

Conclusion and Future Scope

6.1 Conclusion

In today's inustrial scenario a power factor correction becomes an essential tool to avoid the penalties from the utililies. Apart from that low power factor affects on voltage regulation, system capacity and system losses. Therefore industries starts to install an automatic power correction panels for improvement of power factor. A capacitor banks are switched ON and OFF several times in a day which tends to create a transients in the system.

A transient occured during power capacitor switching are eliminated by means of RCSTL network implemented. Transients occurred during the energisation of power capacitors are successfully eliminated by means of coupling transformers, limiting resistor, triac and conrol system. During the energization mode, transients are suppressed through the limiting resistors connected. In steady state mode of operation, secondary of coupling transformer gets short circuited by the triac and thus limiting resistors are bypassed and system runs in steady state.

A hardwre results shows that a proposed RCSTL network considerably improves the power factor of three phase induction motor. Apart from that RCSTL works for three phase resistive load. A multiple switched resistive loads reduces the power factor, but the proposed RCSTL network provides leading capacitive current to maintain the power factor near to unity. Thus proposed RCSTL network is reliable network for improvement of power factor without any transients.

6.2 Future scope

A future scope is to implement the RCSTL network for unbalanced loading conditions. For unbalanced load designing of limiting resistors is not simple. Apart from that for limiting resistor a proper heat sink material is essential otherwise there will be a possibility of fault occurence. Because of capacitive current a system takes more current which may affects on the low rating components. Therefore it is essential to control the current of overall system. A power loss in the circuit at different devices like resistors and coupling transformer needs to be minimized.

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LIST OF PUBLICATIONS ON PRESENT WORK

[1] Gaikwad Yuvraj J., A. R. Thorat "Resistive Capacitive Switching Technique for the Mitigation of Power Capacitor Switching Transients", ICCPEIC, March 2019..

[2] Gaikwad Yuvraj J., A. R. Thorat "Mitigation of Power capacitor Switching Transients with Resistive Capacitor Switching Technique", in review in ECTI transactions on Electrical engineering, Electronics and Communications, Thailand.

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